## COMPLETE LISTING OF THE CLAIMS

This listing of claims will replace all prior versions and listings of claims for this application:

**Listing of Claims:**

1. (Previously presented) A semiconductor assembly comprising:

a first semiconductor die with a top and bottom surface;

at least one second semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said at least one second semiconductor die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one second semiconductor die, said top surface of said first semiconductor die having at least one electrical contact area at a distance outside said perimeter of said at least one second semiconductor die, said at least one second semiconductor die being in electrical communication with said at least one electrical contact area; and

an encapsulating material for encapsulating said at least one second semiconductor die, electrical communication, and at least a portion of said first semiconductor die, said encapsulating material filling a space between said bottom surface of said at least one second semiconductor die and said top surface of said first semiconductor die.

Claims 2-4 (Canceled).

5. (Original) The semiconductor assembly of claim 1, wherein said flowable adhesive material is an epoxy.

6. (Previously presented) The semiconductor assembly of claim 1, wherein said flowable adhesive material covers an area less than or equal to about 90% of said at least one second semiconductor die bottom surface area.

7. (Previously presented) The semiconductor assembly of claim 6, wherein said flowable adhesive material covers an area greater than or equal to about 50 % of said at least one second semiconductor die bottom surface area.

8. (Currently Amended) The semiconductor assembly of claim 1, wherein a distance between said electrical contact area and said perimeter of said at least one second semiconductor die is less than or equal to about 428 microns and greater than zero microns.

9. (Currently Amended) The semiconductor assembly of claim 8, wherein a distance between said electrical contact area and said perimeter of said at least one second semiconductor die is less than or equal to about 200 microns and greater than zero microns.

Claim 10 (Canceled).

11. (Previously presented) The semiconductor assembly of claim 1, wherein said electrical communication is through a wire bond.

12. (Previously presented) The semiconductor assembly of claim 1, wherein said at least one electrical contact area is a bonding pad.

Claims 13-14 (Canceled)

15. (Currently amended) A semiconductor assembly comprising:

a first semiconductor die having a top and a bottom surface;

a second semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second die being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said second semiconductor die such that there is a cavity along at least a portion of said perimeter between said first semiconductor die and said second semiconductor die;

wherein said top surface of said first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of said second semiconductor die, said second semiconductor die being in electrical communication

with said electrical contact area, and wherein a distance between said electrical contact area ~~and~~ said perimeter of said second semiconductor die is less than or equal to about 428 microns and greater than zero microns; and

an encapsulating material for encapsulating said at least one second semiconductor die, electrical communication, and at least a portion of said first semiconductor die, said encapsulating material filling said cavity.

16. (Original) The semiconductor assembly of claim 15, wherein said first semiconductor die is secured to a support structure.

17. (Original) The semiconductor assembly of claim 16, wherein said support structure is a film.

18. (Original) The semiconductor assembly of claim 16, wherein said support structure is a printed circuit board.

19. (Original) The semiconductor assembly of claim 15, wherein said flowable adhesive material is epoxy.

20. (Original) The semiconductor assembly of claim 15, wherein said flowable adhesive material covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area.

21. (Original) The semiconductor assembly of claim 20, wherein said flowable adhesive material covers an area greater than or equal to about 50% of said second semiconductor die's bottom surface area.

Claims 22-40 (Canceled).

41. (Previously presented) A semiconductor assembly comprising:

a support structure having a top surface; and

a first semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said first semiconductor die being secured at its bottom surface to said top surface of said support structure by a compressed flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die such that there is a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material, such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support structure, said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication with said at least one electrical contact area; and

a second semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second semiconductor die being secured at its bottom

surface to said top surface of said first semiconductor die by a compressed flowable adhesive material which does not extend past any one of the sides of said perimeter of said second semiconductor die such that there is a second cavity along at least a portion of said perimeter between said first semiconductor die and said second semiconductor die, said second cavity being filled with said encapsulating material.

42. (Previously presented) A semiconductor assembly comprising:

a support structure having a top surface; and

at least one semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said flowable adhesive material covering an area greater than or equal to about 50% of said at least one semiconductor die's bottom surface area, such that there is a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material, said top surface of said support structure having at least one electrical contact area at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication with said at least one electrical contact area; and

at least a second semiconductor die having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die, said second semiconductor die being secured at

its bottom surface to said top surface of said first semiconductor die by a compressed flowable adhesive material which does not extend past any one of the sides of said perimeter of said second semiconductor die such that there is a second cavity along at least a portion of said perimeter between said first semiconductor die and said second semiconductor die, said second cavity being filled with said encapsulating material,